AMENDMENTS TO THE SPECIFICATION:

Please replace the second full paragraph on page 8 with the following amended paragraph:

First, referring to Fig. 4 showing a block diagram illustrating a semiconductor device in accordance with a preferred embodiment of the present invention, the semiconductor device according to the preferred embodiment includes: a clock buffer 2000 which receives and buffers an external clock signal CLK and outputs the buffered external clock signal CLK as an internal clock signal CLK_I; an clock enable buffer 100 comparing a reference voltage Vref having a constant potential with a clock enable buffer signal CKE and to outputting a first control signal D_out for enabling the clock buffer 2000; and a clock enable buffer signal latch unit 200 which outputs ~~an~~ a buffer enable signal CKE_ON to enable the clock enable buffer 100 using the clock enable buffer signal CKE after a power-up signal is inputted.

Please replace the third full paragraph on page 8 with the following amended paragraph:

Further, a semiconductor device according to the present invention includes a clock enable signal timing controller 300 which passes the first control signal D_OUT and outputs a second control signal OUT to the clock buffer 2000 in response to the buffer enable signal CKE_ON or outputs the second control signal OUT to the clock buffer 2000 by delaying the first control signal D_OUT.

Please replace the first full paragraph on page 9 with the following amended paragraph:

Referring to Fig. 5 showing a circuit diagram illustrating the clock enable buffer in Fig. 4, the clock enable buffer 100 includes: NMOS transistors MN1 and MN2 which have gates receiving the reference voltage Vref and the clock enable buffer signal CKE, respectively; an NMOS transistor MN3 which has a gate receiving the ~~output~~ buffer enable signal CKE_ON and is connected to the NMOS transistors MN1 and MN2 and to a ground voltage level VSS; a PMOS transistor MP1 which has a gate connected to the NMOS transistor MN1 in a diode connection and is connected to a power voltage VDD; a PMOS transistor MP2 which is connected to the power voltage VDD and the NMOS transistor MN2 to form a current mirror together with the PMOS transistor MP1; a PMOS transistor MP3 which has a gate receiving the ~~output~~ buffer enable signal CKE_ON and is connected to the NMOS transistor MN1 and the power voltage VDD; a PMOS transistor MP4 which has a gate receiving the ~~output~~ buffer enable signal CKE_ON and is connected to the NMOS transistor MN2 and the power voltage VDD; and an inverter IN1 for inverting an output signal from the common node of the PMOS transistor MP2 and the NMOS transistor MN2 and outputting the first control signal D_out.

Please replace the paragraph bridging pages 9 and 10 with the following amended paragraph:

Referring to Fig. 6 showing a circuit diagram illustrating the latch unit to latch a clock enable buffer signal in Fig. 4, the clock enable buffer signal latch unit 200 includes: a first clock

enable buffer signal latch unit 210 which is enabled according to the power-up signal pwrup and is disabled according to the ~~output~~ buffer enable signal CKE_ON; and a second clock enable buffer signal latch unit 220 which enables the clock buffer 100 and disables the first clock enable buffer signal latch unit 210 using an output signal S_out from the first clock enable buffer signal latch unit 210. When the external clock signal CLK is inputted into the first clock enable buffer signal latch unit 210 after the first clock enable buffer signal latch unit 210 is enabled, the ~~output~~ buffer enable signal CKE_ON from the second clock enable buffer signal latch unit 220 is continuously in a high voltage level.

Please replace the paragraph bridging pages 10 and 11 with the following amended paragraph:

The first clock enable buffer signal latch unit 210 includes: a NAND gate ND1 receiving the power-up signal pwrup and the ~~output~~ buffer enable signal CKE_ON; a first PMOS transistor MP5 which has a gate receiving the clock enable buffer signal CKE and is connected to the power voltage VDD; a first NMOS transistor MN5 which has a gate receiving the clock enable buffer signal CKE and is connected to the first PMOS transistor MP5; a second NMOS transistor MN4 which has a gate receiving an output signal from the NAND gate ND1 and is connected to both the first NMOS transistor MN5 and a ground voltage level VSS; a second PMOS transistor MP6 which has a gate receiving the output signal from the NAND gate ND1 and is connected to both the power voltage VDD; and a first inverter IN2, which is provided between a common node of the first NMOS transistor MN5 and the first

PMOS transistor MP5 and the second PMOS transistor MP6, to invert a voltage level on the common node of the first NMOS transistor MN5 and the first PMOS transistor MP5.

Please replace the second full paragraph on page 11 with the following amended paragraph:

Fig. 7 is a circuit diagram illustrating the controller to control a timing of the clock enable buffer signal in Fig. 4. The clock enable signal timing controller 300 includes a clock enable signal path selection unit 310, which passes the first control signal D_out to the clock signal latch unit 500 or outputs a delayed signal to the clock signal latch unit 500 by delaying the first control signal D_out, and a path controller 320 to control the transfer path of the first control signal D_out on the clock enable signal path selection unit 310 in response to the buffer enable signal CKE_ON.

Please replace the second full paragraph on page 12 with the following amended paragraph:

The path controller 320 includes: a first PMOS transistor MP9 which has a gate receiving the buffer enable signal CKE_ON; a second PMOS transistor MP10 which has a gate receiving an output signal of the clock enable signal path selection unit 310 and is connected to the first PMOS transistor MP9; a first NMOS transistor MN8 which has a gate receiving the output signal of the clock enable signal path selection unit 310 and is connected to the second PMOS transistor MP10 and the ground voltage level VSS; a first inverter IN6 to

invert a voltage level on the common node of the second PMOS transistor MP10 and the first NMOS transistor MN8 and to produce a first turn-on signal Setb turning on the second transfer gate T2; a second inverter IN7 to invert an output signal of the first inverter IN6 and to produce a second turn-on signal Set turning on the second transfer gate T2; a second delayer 322 which is connected to the second inverter IN7 to and produces a third turn-on signal Setbd turning on the first transfer gate T1; and a third delayer 323 which is connected to the first inverter IN6 to and produces a third turn-on signal Setbd turning on the first transfer gate T1.

Please replace the first full paragraph on page 13 with the following amended paragraph:

When the power-up signal pwrup is not produced after the power voltage VDD is applied to the semiconductor device, that is, when the power-up signal pwrup of a low voltage level is inputted to the clock enable signal latch unit 200, the output of the NAND gate ND1 in the clock enable signal latch unit 200 is in a high voltage level. Accordingly, the NMOS transistor MN4 is turned on. At this time, since the output of the NAND gate ND1 is in a high voltage level and the clock enable buffer signal CKE is in a low voltage level, the buffer enable signal CKE_ON is in a low voltage level.

Please replace the paragraph bridging pages 13 and 14 with the following amended paragraph:

If the clock enable buffer signal CKE goes from low voltage to high voltage and then the high voltage level of the clock enable

buffer signal CKE is inputted into the clock enable signal latch unit 200, the NMOS transistor MN5 is turned on and the output of the inverter IN2 is in a high voltage level to make the buffer enable signal CKE_ON be in a high voltage level. If the buffer enable signal CKE_ON is in a high voltage level, the output of the NAND gate ND1 goes from high voltage level to low voltage level and then the output of the inverter IN2 is set in a high voltage level and, at this time, the buffer enable signal CKE_ON is maintained in a high voltage level, irrespective of the voltage level of the clock enable buffer signal CKE. This high voltage maintenance of the enable signal CKE_ON is made because the power-up signal pwrup, which is applied to the gate of the PMOS transistor MP7 in the second clock enable signal latch unit 220, is kept in a high voltage level. That is, since the power-up signal pwrup is kept in a high voltage level, the PMOS transistors MP7 and MP8 are not turned on simultaneously and the power voltage VDD is not transferred to the inverter IN3 even though the output signal S_out of the inverter IN2 is in a low voltage level.

Please replace the first full paragraph on page 14 with the following amended paragraph:

The clock enable signal latch unit 200 makes the continuous high voltage level signal of the buffer enable signal CKE_ON in response to the first high voltage level of the clock enable signal CKE after the power voltage is applied to the clock enable signal latch unit 200 and the power-up signal is produced.

Please replace the paragraph bridging pages 14 and 15 with the following amended paragraph:

Referring again to Fig. 5, the clock enable buffer 100 is enabled according to the buffer enable signal CKE_ON from the clock enable signal latch unit 200 and compares the clock enable buffer signal CKE with the reference voltage Vref. According to the result of the comparison, the first control signal D_out is outputted. The first control signal D_out is passed through the clock enable signal timing controller 300 and it is outputted as the second control signal OUT in the clock enable signal timing controller 300. The clock signal latch unit 500 receiving the second control signal OUT outputs the internal clock signal CLK_I.

Please replace the first full paragraph on page 15 with the following amended paragraph:

In the semiconductor devices according to the present invention, the buffer enable signal CKE_ON is produced after the power-up signal pwrup has been inputted and, since the clock enable buffer 100 is enabled according to the buffer enable signal CKE_ON, the first control signal D_out is not outputted by an erroneous generation of the reference voltage Vref and the clock enable buffer signal CKE after the initial voltage is applied to the semiconductor device. Namely, the present invention can get rid of an erroneous operation, in which the clock enable buffer signal CKE is acknowledged as a high voltage level signal with respect to the reference voltage Vref because the reference voltage Vref and the clock enable buffer signal CKE are abnormally produced at the

initial operation time of the semiconductor device.

Please replace the paragraph bridging pages 15 and 16 with the following amended paragraph:

Referring again to Fig. 7, since the clock enable signal latch unit 200 receives the clock enable buffer signal CKE and outputs the buffer enable signal CKE_ON and the clock enable buffer 100 produces the first control signal D_out to enable the clock buffer 2000 using the buffer enable signal CKE_ON, a set-up timing margin of the clock enable buffer signal CKE may decrease in comparison with the clock signal CLK. For this reason, the clock enable signal timing controller 300 is provided to control output paths of the first control signal D_out which is produced by the clock enable buffer signal CKE.

Please replace the second full paragraph on page 16 with the following amended paragraph:

In the path controller 320 of the clock enable signal timing controller 300, when the buffer enable signal CKE_ON is in a low voltage level and the second control signal OUT is in a low voltage level, the output signal of the inverter IN6 is in a low voltage level and the output signal of the inverter IN7 is in a high voltage level. Accordingly, since the second transfer gate T2 is turned on and the first transfer gate T1 is turned off, the first control signal D_out is passed through the second transfer gate T2 to form the second control signal OUT and the second control signal OUT is outputted to the clock buffer 2000.

Please replace the first full paragraph on page 17 with the following amended paragraph:

On the other hand, the inverter IN4 and the NMOS transistor MN7 in the clock enable signal path selection unit 310 makes the input terminal thereof be in the ground voltage level at the initial time the power-up signal pwrup is kept in a low voltage level. Namely, in order to overcome a deficient set-up margin when the buffer enable signal CKE_ON is produced and the clock enable buffer 100 is first enabled at the initial operation of the semiconductor device, the first control signal D_out, which is first inputted into in the clock enable signal timing controller 300, is fast outputted as the second control signal OUT after the buffer enable signal CKE_ON is activated in a high voltage level. Thereafter, the subsequent input signals of the first control signal D-out are delayed and the delayed signals are outputted ad the second control signal OUT.